# TRAINING DESCRIPTION

## Sommario



**Leading Edge**
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**Sede Operativa**
Via Abruzzo 6
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# Board Level Signal/Power Integrity Workshop

The complexity of today's designs is such that PCB designers are required to know the reasons behind the electrical effects happening on a board when a high-speed signal travels along a trace. This 1 day workshop (with theory sessions and examples run with commercial software solutions) will give the basics of how to estimate, calculate, and simulate signal integrity issues before they arise and is intended for engineers who want to know about reflections, cross-talk, power noise and Electromagnetic Emissions and how to avoid/correct them.

# TCL/TK

These days most EDA tools use a TCL based command line interface and many use Tk for the graphical interface. This one-day theory and practice course helps you unleash the power of TCL/TK and improve your scripting abilities to get the most from your EDA tools.

# Introduction to Perl

This 2-day class will introduce the student to the Perl programming language. Upon completion of this class, the student will be able to write useful Perl programs to automate operating system tasks and perform sophisticated text manipulation. Students will also have a brief introduction to Perl's GUI capabilities through Perl/Tk. The format of the class is mixed lecture/lab, with lab exercises immediately following each major topic. The lab exercises are intended to reinforce the preceding lecture topic(s) and are designed to be directly applicable in an EDA context.

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# SystemVerilog for Verification

This 4-day course is aimed at experienced Verification engineers who wish to learn about verification with SystemVerilog. The course stresses a methodology for implementing these features in your verification environment. This course is taught for all the leading simulators although not all simulators will support every feature immediately. The course is a consistent mix of lecture and lab-exercises. Targeted quizzes and labs are designed to reinforce the course material. Some of this class overlaps our SystemVerilog for Designers course.

# SystemVerilog for Design

A 2-day course with an optional 1-day introduction to Verilog for designers unfamiliar with the Verilog language. The course is aimed at RTL designers who wish to learn about the new features of SystemVerilog for RTL design including the use of concurrent assertions for verification of functional behavior. Attendees will learn the new synthesizable constructs and features available in SystemVerilog. Synthesis tools are not required.

# SystemVerilog Assertions (SVA)

Assertion Based Verification is becoming a cornerstone of good design and verification practice. SystemVerilog is one of the first languages to feature a 100% native temporal assertion syntax, making it extremely well integrated with the language. The course stresses a methodical approach to learning and developing good coding style. Although the content of this class overlaps the final day of our SystemVerilog for Design and SystemVerilog for Verification courses, both SVA and our course are applicable to Verilog projects with no other SystemVerilog content.

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# Introduction to Universal Verification Methodology (UVM)

This course is for engineers interested in developing SystemVerilog verification environments using the latest Universal Verification Methodology (UVM). The course starts with the basic UVM testbench structure then builds on this to show techniques for building powerful and efficient UVM testbenches. The course is a consistent mix of lecture and lab-exercises. Targeted quizzes and labs are designed to reinforce the course material.

# Introduction to Verilog for RTL Design

This course teaches designers to write efficient, accurate RTL code for synthesis as well as basic test-benching and verification techniques and is intended for designers who are new to Verilog and who wish to become familiar with the language with a particular emphasis on writing RTL code for synthesis. We also cover how to construct testbenches for unit level verification of your RTL code.

# Introduction to VHDL for RTL Design

This course teaches designers to write efficient, accurate RTL code for synthesis as well as basic test benching and verification techniques and is intended for designers who are new to VHDL. It focuses on teaching good RTL coding style for synthesis but also discusses basic test benching and verification techniques.

# Advanced VHDL

This course emphasizes behavioral techniques, testbench strategies and design management and is aimed at experienced VHDL users who wish to take their use of the language to a higher level.

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## Advanced VHDL for Design

A 3-day course introducing VHDL language features which are not commonly known or used. This class is aimed at experienced VHDL users who wish to take advantage of the lesser known aspects of the VHDL language to create reliable, re-usable design units in a standardized manner. A pre-requisite for this course is the Introduction to VHDL course or equivalent experience.

# IPC Courses

## IPC - CID Certification (Certified Interconnect Designer)

CID certification is a **universally recognized** professional credential in the electronic industry. The CID course was developed by IPC to provide the necessary tools for the design of circuit boards. It is intended not to the designer but to anyone involved with the design, development and manufacture of PCBs at any level, from sales and management to purchasing and QA.

## IPC – CID+ Certification (Advanced Interconnect Designer Certification)

The CID+ program is designed for those who design PCB's as well as those who need knowledge of the IPC Design Standard. CID+, Enhanced Certified Interconnect Designer is a valuable professional credential recognized throughout the electronics industry based on several critical IPC documents that link design principles to the end product use of the printed board assembly and is open to whom has the CID certification.

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# IPC - A - 600 Certification, Acceptability of Printed Boards

This is a Certified Training Program which covers the acceptance criteria for Printed Circuit Boards. Based on the latest revision of "IPC-A-600 standard", which provides photographs and illustrations of the target, acceptable and nonconforming conditions that are either internally or externally observable on bare printed boards.

This training is a theoretical course which is suitable for any person who is responsible for quality and reliability PCBs. It is intended for people who work as inspectors at suppliers of printed circuit boards (PCB suppliers) and for who is responsible of the incoming inspection, or for the PCB assemblers, or for the PCB user.

# IPC - A - 610 Certification, Acceptability of Electronic Assemblies

The 610 Training is a Certified Training Program which covers acceptance criteria for all Electronics Assemblies. It is based on the latest revision of "IPC-A-610 standard", and is a must-have for inspectors, operators and others with an interest in the acceptance criteria for electronic assemblies.

# IPC - A - 620 Certification, Requirements and Acceptance for Cable and Wire Harness Assemblies

**I**PC/WHMA-A-620, Requirements and Acceptance for Cable and Wire Harness Assemblies, is the industry standard for cable and wire harness fabrication and installation. The IPC/WHMA-A-620 Certified IPC Specialist (CIS) course is designed to improve individual discrimination skills, which means to improve accuracy of discriminating between an acceptable or not acceptable cable or wire harness assembly per the IPC/WHMA-A-620 document. This training is theoretical and is suitable for any person who is responsible for quality and reliability of Cable & Wire Harness Assemblies.

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## IPC – J- STD - 001 Certification, Requirements for Soldered Electrical & Electronic Assemblies

The IPC J-STD-001 describes the materials, methods and verification criteria for producing high-quality, soldered, leaded and lead-free interconnections, and emphasizes the process control needed for their achievement. Working according to the standard, and having staff properly is the way to gain a higher quality manufacturing level. The course covers the material and process requirements for electrical/electronic assembly welds and is a practical and theoretical course. This standard is aimed at anyone needing to understand whether a soldered joint is acceptable, such as: process engineers, assembly operators, quality and inspection staff, as well as anyone responsible for the quality and reliability of soldered assemblies.

# Intel® FPGA Technical Training Courses

**For more information, visit our website: https://www.leading-edge.it/en/our-services/cad-software-training/**

### Quartus Prime

The Intel® Quartus® Prime Software: Foundation

The Intel® Quartus® Prime Software: Foundation for Xilinx® Vivado® Design Suite Users

The Intel® Quartus® Prime Software: Timing Analysis with Timing Analyzer

The Intel® Quartus® Prime Software: Pro Edition Features for High-end Designs

The Intel® Quartus® Prime Software: Foundation

## SoC Series

Introduction to the Platform Designer System Integration Tool

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# OpenCL Series

Introduction to OpenCL™ Programs for Intel® FPGAs

Developing a Custom OpenCL™ BSP

# DSP Builder for Intel® FPGAs

Designing with DSP Builder for Intel® FPGAs

Designing with DSP Builder (advanced)

# HDL Languages

Introduction to Verilog

Advanced Verilog Design Techniques

Introduction to VHDL

Advanced VHDL Design Techniques

## Methodology Courses

Advanced Timing Analysis with Timing Analyzer

Timing Closure with Intel® Quartus® Prime Pro Software

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