Board Level Signal/Power Integrity Workshop

The complexity of today designs is such that PCB designers are required to know the reasons behind the electrical effects happening on a board when a high speed signal travels along a trace.
This 1 day workshop (with theory sessions and examples run with commercial software solutions) will give the basics of how estimate, calculate, and simulate signal integrity issues before they arise and is intended for engineers who want to know about reflections, cross-talk, power noise and Electromagnetic Emissions and how to avoid/correct them.

TCL/TK

These days most EDA tools use a TCL based command line interface and many use Tk for the graphical interface. This one day theory and practice course helps you unleash the power of TCL/TK and improve your scripting abilities to get the most from your EDA tools.

Liberty

The open standard Liberty format is used by most synthesis and timing analysis tools for functional, timing and power information of standard cell library elements. This three day course is intended for engineers who want to have a deep understanding of the syntax and how the information is used by various EDA tools.

IPC CID

This professional development program provides objective evaluation of core competencies in design, based upon industry standards rather than specifications of just one company. Courses enhance and assess technical knowledge: how to transform an electrical circuit description into a reliable PCB design that can be manufactured, assembled, tested.

SystemVerilog for Verification

The course stresses a methodology for implementing these features in your verification environment.
This course is taught for all the leading simulators although not all simulators will support every feature immediately.
The course is a consistent mix of lecture and lab-exercises. Targeted quizzes and labs are designed to reinforce the course material.
Some of this class overlaps our SystemVerilog for Designers course.

SystemVerilog Assertions (SVA)

Assertion Based Verification is becoming a cornerstone of good design and verification practice. SystemVerilog is one of the first languages to feature a 100% native temporal assertion syntax, making it extremely well integrated with the language. The course stresses a methodical approach to learning and developing good coding style.

Although the content of this class overlaps the final day of our SystemVerilog for Design and SystemVerilog for Verification courses, both SVA and our course are applicable to Verilog projects with no other SystemVerilog content.

Introduction to Universal Verification Methodology (UVM)

This course is for engineers interested in developing SystemVerilog verification environments using the latest Universal Verification Methodology (UVM).

Introduction to Verilog for RTL Design

This course teaches designers to write efficient, accurate RTL code for synthesis as well as basic testbenching and verification techniques and is intended for designers who are new to Verilog and who wish to become familiar with the language with a particular emphasis on writing RTL code for synthesis. We also cover how to construct testbenches for unit level verification of your RTL code.

Introduction to VHDL for RTL Design

This course teaches designers to write efficient, accurate RTL code for synthesis as well as basic testbenching and verification techniques and is intended for designers who are new to VHDL. It focuses on teaching good RTL coding style for synthesis but also discusses basic testbenching and verification techniques.

Advanced VHDL

This course emphasizes behavioral techniques, testbench strategies and design management and is aimed at experienced VHDL users who wish to take their use of the language to a higher level.