

Board Level Signal Integrity

The complexity of today designs is such that PCB designers are required to know the reasons behind the electrical effects happening on a board when a high speed signal travels along a trace.

This 3 days theory and practice course will give the basics of how estimate, calculate, and simulate signal integrity issues before they arise and is intended for engineers who want to know about reflections, cross-talk, power noise and Electromagnetic Emissions and how to avoid/correct them.

TCL/TK

These days most EDA tools use a TCL based command line interface and many use Tk for the graphical interface. This one day theory and practice course helps you unleash the power of TCL/TK and improve your scripting abilities to get the most from your EDA tools.

Liberty

The open standard Liberty format is used by most synthesis and timing analysis tools for functional, timing and power information of standard cell library elements. This three day course is intended for engineers who want to have a deep understanding of the syntax and how the information is used by various EDA tools.