

CONSORTIUM

Nangate A/S, based in Copenhagen, Denmark is the project coordinator. According to Nangate's CEO, Ole Chr. Andersen, participation in the project "will enable Nangate to further strengthen and escalate our existing technology partnership and customer relations that focus on introducing regular layout optimised capabilities to our present range of advanced cell library and design optimisation EDA tools".

Consortium partners include Europe's largest IDM, **STMicroelectronics**; **Thales** (France), which is the European global technology leader for the aerospace, space, defence, security and transportation markets; and **imec** (Belgium), which performs world-leading research in nanoelectronics. Three leading universities, **Politecnico di Milano** (Italy), **Universitat Politècnica de Catalunya** (Spain) and **Universidade Federal do Rio Grande do Sul** (Brazil) will bring significant and highly specialised technology contributions to the joint research. The final partner, **Leading Edge**, is participating in its capacity as a consultancy company specialising in the introduction of innovative EDA technologies to the European marketplace.

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The **Synaptic** project addresses Objective ICT-2009.3.2: "Design of Semiconductor Components and Electronic Based Miniaturised Systems" by development of "methods and tools to cope with the design challenges in the next generations of technologies" and focuses on the objective "design for manufacturability taking into account increased variability of new processes".

In particular, the project targets the optimisation of manufacturability and the reduction of systematic variations in nanometer technologies through exploitation of **regularity at the architectural, structural, and geometrical levels**. We propose the creation of a *methodology* and associated *suite of design tools* which extract regularity at the architectural and structural level and automate the creation of regular compound cells which implement the functionality of the extracted templates.

The cell creation will employ **Restricted Design Rules** (RDR's) and other regularity techniques at the geometrical level to maximise manufacturability and reduce systematic variations. Since the majority of designs in the nanometer regime employ some form of *embedded* SRAM, the project will include a study of the effects of RDR's on SRAM in terms of performance and manufacturability and the subsequent definition of a set of RDR's, which allow manufacturability optimisation for logic functions while remaining compatible with SRAM *design rules*.



SYNAPTIC

SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms



Duration: 36 months

Start: November 2nd, 2009

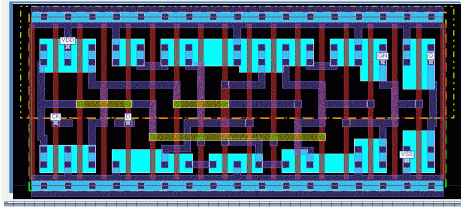
Theme: – ICT-2009.3.2: Design of semiconductor components and electronic based miniaturised systems

<http://www.synaptic-project.eu>

PROJECT MOTIVATIONS

Through use of a more restrictive set of layout patterns with predictable layout neighbourhood, variability caused by the physical limitations of current industrial lithography techniques can be reduced and manufacturing yield can be improved. An additional benefit of this approach is that it eases RET computation and hence reduces mask generation complexity. However, in particular for implementation of random logic with state-of-the-art automated implementation methodologies, the layout restrictions lead to loss of density of the logic cell libraries and a reduced block-level gate density when compared with traditional methodology utilising cell libraries with more complex layout patterns. For this reason, complex patterned logic cells followed by advanced mask processing steps have continued to be the dominating approach.

With the introduction of advanced process nodes at 32nm and below, new and significant layout restrictions lead to a more regular layout style being applied for the fundamental logic cells. The trend for more regular layout will continue as scaling advances. To enable technology scaling to remain attractive, it is necessary to counter the negative effects of regularity restrictions on logic density. It is therefore critically important to focus research efforts on *exploring and developing innovative design techniques and methodologies, along with associated CAD tools and logic cell libraries*, which remove the limitations in design implementation effectiveness associated with technology scaling and advanced sub-wavelength lithography.



TECHNICAL ASPECTS

The consortium behind the **Synaptic** project spans a range of technology companies and research institutions, each with a unique specialisation, allowing them to set up a unique joint research project aiming to develop a revised design methodology in which the concept of regularity is propagated through all abstraction levels: architectural, logic and physical layout.

- From an **architectural** point of view, the advantages of the proposed methodology include the ability to exploit step and repeat approaches employing complex logic cells and complex logic building blocks, thus providing greater predictability of design performance and enabling comprehensive early architecture exploration. Reliance upon complex logic cells and logic building blocks realised by regular layout patterns reduces sensitivity to process variations, improves performance predictability and enables tighter design margins.
- From a **logic** design point of view, the advantages include the creation of logic cell libraries targeted to design requirements, thus improving performance and performance predictability.
- From a **physical** design point of view, this approach will enable the use of lower-cost lithography techniques as compared to complex patterned logic cell approaches while achieving the same yield. This makes it cost-effective to use more advanced lithography techniques on large SoC designs, thus enabling the use of more

advanced semiconductor technologies. Layout regularity will further increase the predictability of the design as well as reducing excessively small CD transistors which add to leakage problems.

CONTACTS

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