

Concept Engineering's RTLvision Debugger and Viewer to Power Real Intent's Verification Solutions

Multi-year OEM agreement outlines integration with Real Intent's iDebug tool to enhance problem visualization, deliver higher-quality designs and speed time to market

Freiburg, Germany – January 23, 2017 – Concept Engineering, specialists in visualization and debugging technology for electronic circuits and systems, today announced a multi-year OEM agreement with Real Intent, a leading provider of SoC and FPGA sign-off verification solutions, in which Real Intent will integrate and use Concept Engineering's RTLvision® debugger and viewer with the Real Intent Meridian™ and Ascent™ suites of RTL and gate-level analysis tools. Real Intent's version of RTLvision is called iVision.

The new integration with Real Intent's iDebug™ analyzer helps design engineers more easily understand and fix critical RTL and gate-level design issues including clock-domain crossing (CDC), Reset Domain Crossing (RDC), X-propagation and functional problems; deliver higher-quality designs; and reduce time to market.

iVision provides easy RTL debugging and fast visualization of RTL code and analysis waveforms, so that engineers can quickly fix problems to deliver better product quality. iVision's integration with Real Intent's advanced analysis capabilities enables circuit designers to:

- See detailed schematics of violated circuit paths, design hierarchy, clock and reset logic for debug drill down
- Visualize waveforms from Ascent and Meridian analysis engines to expose circuit behaviors
- Efficiently pinpoint functional logic, clock and reset problems for fast debug
- Easily cross-probe from schematic to the HDL source code to quickly fix detected problems.

"The Ascent and Meridian products from Real Intent analyze and verify giga-scale RTL designs," said Ramesh Dewangan, vice president of Marketing and Product Strategy at Real Intent. "We find that Concept Engineering's RTLvision technology delivers the fastest visualization performance and has the most efficient database for capturing design data in the market today. Integrating its capabilities

to Real Intent's iDebug environment to uncover critical problems during RTL signoff and early functional verification means our customers will have an even faster debug experience and save hours of development time."

"Real Intent is a leading EDA company with a comprehensive suite of RTL and gate-level static signoff solutions," said Gerhard Angst, CEO and president of Concept Engineering. "We are pleased to help Real Intent's customers more quickly solve design problems such as clock domain crossing, reset domain crossing, linting, X-propagation, constraints and exception verification with our market leading visualization technology."

About Concept Engineering

Concept Engineering is a privately-held company based in Freiburg, Germany, that provides visualization and debugging technology for electronic circuits and systems, including automatic schematic generation technology for all major design levels. The company's technology helps electronic design engineers to easily understand, debug, optimize and document electronic designs. Concept Engineering's software technology is used in many fields in the EDA market, including: RTL development, IP reuse, ASIC and SoC design, FPGA design, analog/mixed-signal design, logic synthesis, design verification, test automation, post-layout analysis, debugging and visualization at system level, RTL level, netlist level and transistor level.

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Press Contact

Cayenne Communication LLC for Concept Engineering in North America:

Michelle Clancy, michelle.clancy@cayennecom.com, +1.415.682.4552

Concept Engineering GmbH:

Gerhard Angst, gerhard@concept.de, +49.761.470940

Company Contact

Concept Engineering GmbH· Bötzingler Str. 29· 79111 Freiburg· Germany

Tel: +49-761- 47094-0· Fax: +49-761- 47094-29· Email: info@concept.de· <http://www.concept.de>